REMARKS

Summary of the Amendment

Upon entry of the present Amendment, Claims 27 and 32 will have been amended. Accordingly, Claims 27-41 remain pending in the present application. By the present Amendment and Remarks, Applicant submits that the objections and rejections have been overcome, and respectfully requests reconsideration of the outstanding Office Action and allowance of the present application.

Summary of the Office Action

In the subject Office Action, Claims 27-37 and 41 are rejected under 35 U.S.C. §102(e) as being anticipated by the art of record, and Claims 38-40 are rejected under 35 U.S.C. §103(a) as being unpatentable over the art of record.

Traversal of Rejection under 35 U.S.C. §102(e)

In re YAGI

Applicant respectfully traverses the rejection of Claims 27-36 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,201,292 to Yagi et al. [hereinafter "YAGI"].

The Examiner submits that YAGI discloses a semiconductor device (Figs. 7 and 12) that contains a flat paddle 24 having an upper surface that is partially etched which extends about the periphery, a plurality of leads 22 arranged adjacent to the paddle 24, at least some of the leads 22 each having a lower surface, an upper surface and a lead lock comprising at least one disk shaped protrusion (the circle shaped element in Fig. 12), which is partially defined by the upper surface of the lead and includes a bottom surface positioned between the upper and lower surfaces of the lead, a semiconductor chip 27 having a lower surface mounted on the paddle 24 by a thermally conducting adhesive 26, conductive wires 28 each electrically connecting respective ones of the leads 22 to the chip, a resin encapsulant 29 defining the bottom surface and at least partially encapsulating the chip 27, lead lock of the leads 22 and the conductive wires 28 wherein a portion of the lower surface of each of the leads 22 is exposed at the bottom of the encapsulant 29, a plating layer applied to a lower

surface of the leads [bond pad(22b)], and a plurality of solder balls 30 being attached to the lower surface of the leads 22 and serving as an external input/output terminal.

A Review of YAGI (Revisited)

Figure 7 is a cross-sectional view of a resin-sealed semiconductor device 21' which includes a plurality of terminal portions 22 arranged two-dimensionally in two rows substantially on a plane and electrically independent of one another. A rectangular die pad 24 is disposed in a middle portion of the arranged terminal portions 22. The bottom surface of semiconductor element 27 is attached via an adhesive 26 onto a top surface of die pad 24. The terminal portion 22 includes an inner terminal 22A and an outer terminal 22B. The top of the inner terminal 22A includes a silver plating layer 23. Wires 28 electrically connect terminals 27a of the semiconductor element 27 to the terminals 22 at the silver plated portions 23. The terminal portions 22, the die pad 24, the semiconductor element 27 and the wires 28 are sealed by a sealing member 29 in such a manner that portions of the outer terminals 22B and the lower side of the die pad 24 are exposed to the outside. It is further noted that the semiconductor device 21' is constituted by forming outer electrodes 30 of solder materials onto the exposed surfaces 22b of the outer terminals 22B of the semiconductor device 21'. This resin-sealed semiconductor device 21' is considered a ball grid array device (BGA).

Figures 11 and 12 of YAGI disclose a semiconductor device 41 which includes a plurality of terminal portions 42 arranged electrically independent of one another two dimensionally and substantially in a plane. A die pad 44 is disposed in a substantially middle portion of the arranged terminal portions 42. Die pad 44 has a rectangular surface configuration. It is noted that a semiconductor element 47 is mounted via an adhesive 46 onto the lower surface of die pad 44. Therefore, the aforementioned embodiment shown in Figures 11 and 12 is different from the semiconductor package shown in Figure 7 because the semiconductor element 47 is mounted underneath the die pad 44 as compared to Figure 7 where the semiconductor element 27 is mounted on top of the die pad 24. The terminal 42 has an inner terminal 42A and an outer terminal 42B. An upper surface 42a of each terminal 42 is provided with silver plating 43. The terminal portions 42, the die pad 44, the

semiconductor element 47 and the wires 48 are sealed by a sealing member 49 in such a manner that the outer terminals 42B are partially exposed to the outside.

In re Independent Claims 27 and 32 (and Dependent Claims 28-31 and 33-36)

Applicant's independent Claim 27 recites, *inter alia*, . . . at least one disk-shaped protrusion which is partially defined by the upper surface of the lead and includes ***a bottom disk surface positioned between the upper and lower surfaces of the lead***. . .

Similarly, Applicant's independent Claim 32 recites, *inter alia*, . . . at least one disk-shaped protrusion which is partially defined by the upper surface of the lead and includes ***a bottom disk surface positioned between the upper and lower surfaces of the lead***. . .

Applicant respectfully submits that YAGI does not teach or suggest at least the aforementioned features of Claims 27 and 32. Instead, that portion of each YAGI terminal portion or lead 42 which the Examiner characterizes as the "circle shaped element in Fig. 12" includes the inner terminal 42A which defines the upper surface 42a, and the outer terminal 42B which defines the lower surface 42b (see Figure 11). It is the lower surface 42b is the lowermost surface of the terminal portion 42 and is exposed in the sealing member 49 such that a solder ball 50 may ultimately be applied thereto. Thus, as in readily apparent from Figures 11 and 12 of YAGI, the lower surface 42b, which is arguably that surface which is most analogous to the bottom disk surface recited in each of Claims 27 and 42, is ***not*** positioned between the upper and lower surfaces 42a, 42b of the terminal portion 42. Rather, the lower surface 42b ***is*** the lower surface of the terminal portion 42. Figure 12 of YAGI makes clear that portion of the terminal portion 42 extending from the inner and outer terminals 42A, 42B to the side surface of the sealing member 49 is not disk shaped, and does not have a width exceeding that of the remainder of the terminal portion 42.

For the foregoing reasons, and because YAGI fails to disclose the above-noted features of the present invention, Applicant submits that YAGI fails to disclose each and every feature of the present invention as recited in independent Claims 27 and 32.

Accordingly, Applicant submits that the Examiner has failed to provide an adequate evidentiary basis to support a rejection under 35 U.S.C. §102(e) and that the rejection of independent Claims 27 and 32 is improper and should be withdrawn.

Applicant further submits that dependent Claims 28-31 and 33-36 are allowable at least for the reason that these claims depend from respective ones of allowable independent Claims 27 and 32 and recite additional features that further define the present invention.

In re OKUMURA

Applicant respectfully traverses the rejection of Claims 37 and 41 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 5,942,794 to Okumura et al. [hereinafter "OKUMURA"].

The Examiner submits that OKUMURA discloses a semiconductor device (Fig. 11) that contains a flat paddle 102 having an upper surface that is partially etched which extends about the periphery, a plurality of leads 104 arranged adjacent to the paddle 102, at least some of the leads 104 having a lower surface and a lead lock 104a comprising inclined side walls having an increased width defined therebetween in an upward direction from the lower surface, a semiconductor chip 103 having a lower surface mounted atop the paddle 102, conductive wires 105 electrically connecting respective ones of the leads 104 to the chip 103 and a resin encapsulant 106 defining the bottom surface and at least partially encapsulating the chip 103, lead lock of the leads 104 and the conductive wires 105 wherein a portion of the lower surface of each of the leads 104 is exposed at the bottom of the encapsulant 106.

A Review of OKUMURA (Revisited)

Figure 11 of OKUMURA discloses a conventional single-sided plastic encapsulated semiconductor device. A semiconductor chip 103 is mounted on a die pad 102 of the lead frame 101. An electrode of the semiconductor chip 103 is electrically connected to inner leads 104 of the lead frame 101 via metal wires 105. The semiconductor chip 103, die pad 102, inner leads 104, and metal wires 105 are sealed with a sealing resin 106. Tip portions 104a of the inner leads 104 of the lead frame 101 are formed to have tapered profiles to exhibit sufficient adhesion to sealing resin 106. It is further noted that the tip portions 104a of the inner leads 104 are formed to have tapered profiles by mechanical or chemical processing.

Independent Claim 37 (and Dependent Claim 41)

Applicant's independent Claim 37 recites, *inter alia*, . . . at least some of the leads each having a lower surface and a lead lock comprising inclined ***side walls*** having an increased width defined therebetween in an upward direction from the lower surface; . . . Applicant respectfully submits that OKUMURA does not teach the aforementioned features.

As shown in the Applicant's specification, the lead in Figure 4 has an inverted-trapezoidal cross-section. That is, each lead has inclined ***side walls*** serving as lead lock 14. Since each lead lock 14 has a tapered structure increasing in width as it extends inwardly from the bottom of the resin encapsulant 106, there is no possibility for the leads to be separated form the resin encapsulant 106 even when they receive cutting impact during a singulation process.

On the other hand, the prior art semiconductor device shown in Figure 11 of OKUMURA does not teach what is recited above in Applicant's independent Claim 37. In particular, OKUMURA does not teach, *inter alia*, each lead lock comprising inclined ***side walls*** (plural) having an increased width defined therebetween in an upward direction from the lower surface. *Instead, the OKUMURA inner leads 104 appear to have only* ***one*** *tapered side on the inner tip of the inner lead 104.* Thus, Figure 11 of OKUMURA does not teach inclined ***side walls*** on both sides of the lead as is taught in the Applicant's invention as recited in independent Claim 37.

For the foregoing reasons, OKUMURA fails to disclose the above noted features of the present invention. Therefore, Applicant submits that OKUMURA fails to disclose each and every feature of the present invention as recited in independent Claim 37.

Accordingly, Applicant submits that the Examiner has failed to establish an adequate evidentiary basis to support a rejection under 35 U.S.C. § 102(e) and that the rejection of independent Claim 37 is improper and should be withdrawn.

Applicant further submits that dependent Claim 41 is allowable at least for the reason that this claim depends from allowable independent Claim 37 and recites additional features that further define the present invention.

Traversal of Rejection under 35 U.S.C. §103(a)

Applicant respectfully traverses the rejection of Claims 38-40 under 35 U.S.C. §103(a) as being unpatentable over OKUMURA in view of YAGI.

The Examiner submits that OKUMURA discloses all of the limitations except for a plurality of solder balls and adhesive on the paddle and chip. The Examiner further submits that YAGI discloses a paddle 24, a plurality of leads 22 arranged adjacent to the paddle, a semiconductor chip 27 having a lower surface and mounted on the paddle by a thermally conducting adhesive 26, conductive wires 28 each electrically connecting respective ones of the leads to the chip, a resin encapsulant 29 defining the bottom surface and at least partially encapsulating the chip, lead lock of the leads and the conductive wires wherein a portion of the lower surface of each of the leads is exposed at the bottom of the encapsulant, a plating layer applied to the lower surface of the leads [bond pad (22b)] and a plurality of solder balls 30 being attached to the lower surface of the leads and serving as an external input/output terminal. The Examiner further submits that solder balls were formed on the bottom of the leads for electrical connection to the outer circuit substrate (column 5, lines 13-16). The Examiner concludes that it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device of OKUMURA by incorporating solder balls to the end of the leads to form electrical connections to the outer circuit substrate as taught by YAGI.

Independent Claim 37 (Dependent Claims 38-40)

As discussed above, Applicant submits that independent Claim 37 is allowable because OKUMURA does not teach, *inter alia*, . . . at least some of the leads each having a lower surface and a lead lock comprising inclined ***side walls*** having an increased width defined therebetween in an upward direction from the lower surface; . . .

Applicant further submits that YAGI does not teach, *inter alia*, . . . at least some of the leads each having a lower surface and a lead lock comprising inclined side walls having an increased width defined therebetween in an upward direction from the lower surface; . . .

Therefore, whether OKUMURA or YAGI are considered individually or in combination, and even if the aforementioned references are properly combined, the invention

recited in independent Claim 37 still does not result from the Examiner's proposed modification of OKUMURA in view of YAGI.

Applicant further submits that dependent Claims 38-40 are allowable at least for the reason that these claims depend from allowable independent Claim 37 and because these claims recite additional features that further define the present invention.

Accordingly, Applicant submits that the Examiner has failed to provide an adequate evidentiary basis to support a rejection under 35 U.S.C. §103(a) and that the present rejection of dependent Claims 38-40 is improper and should be withdrawn.

CONCLUSION

Applicant respectfully submits that each and every pending claim of the application meets the requirements for patentability and respectfully requests that the Examiner indicate the allowance of such claims.

In view of the foregoing, it is submitted that none of the references of record when considered individually or in any proper combination thereof, anticipate or render obvious the Applicant's invention as recited in Claims 27-41. The applied references of record have been discussed and distinguished, while the significant claimed features of the present invention have been pointed out.

Further, any amendments to the claims which have been made in this response and which have not been specifically noted to overcome a rejection based upon prior art, should be considered to have been made for a purpose unrelated to patentability, and no estoppel should be deemed to attach thereto.

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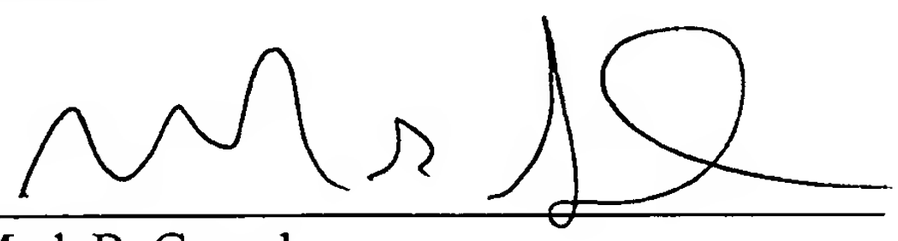
Respectfully submitted,

Date: 5/6/05 By: 

Mark B. Garred
Registration No. 34,823
STETINA BRUNDA GARRED & BRUCKER
75 Enterprise, Suite 250
Aliso Viejo, California 92656
Telephone: (949) 855-1246
Fax: (949) 855-6371

Customer No.: 007663

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